



Subject card

Subject name and code	Computer Architecture, PG_00047659						
Field of study	Informatics						
Date of commencement of studies	October 2021	Academic year of realisation of subject			2022/2023		
Education level	first-cycle studies	Subject group			Obligatory subject group in the field of study		
Mode of study	Full-time studies	Mode of delivery			at the university		
Year of study	2	Language of instruction			Polish		
Semester of study	3	ECTS credits			6.0		
Learning profile	general academic profile	Assessment form			exam		
Conducting unit	Department of Computer Architecture -> Faculty of Electronics, Telecommunications and Informatics						
Name and surname of lecturer (lecturers)	Subject supervisor	dr inż. Tomasz Dziubich					
	Teachers	dr inż. Tomasz Dziubich dr inż. Marcin Narloch mgr inż. Tymoteusz Cejrowski mgr inż. Karol Draszawka					
Lesson types and methods of instruction	Lesson type	Lecture	Tutorial	Laboratory	Project	Seminar	SUM
	Number of study hours	30.0	15.0	15.0	0.0	0.0	60
	E-learning hours included: 0.0						
Learning activity and number of study hours	Learning activity	Participation in didactic classes included in study plan	Participation in consultation hours		Self-study		SUM
	Number of study hours	60	7.0		83.0		150
Subject objectives	The aim of the course is to provide knowledge of the concepts related to the computer architecture and knowledge of the basic mechanisms of processors at the ISA level, and to present the latest trends in the construction of the processors.						
Learning outcomes	Course outcome	Subject outcome			Method of verification		
	[K6_U05] can plan and conduct experiments related to the field of study, including computer simulations and measurements; interpret obtained results and draw conclusions	Student will differentiate working mode of CPU (real and protected mode), and has the ability of development of secure and safety interrupt routine.			[SU1] Assessment of task fulfilment		
	[K6_U02] can perform tasks related to the field of study in an innovative way as well as solve complex and nontypical problems, applying knowledge of physics, in changing and not fully predictable conditions	Student will demonstrate knowledge of assembly programming and testing; Student will demonstrate knowledge of integration low-level and high-level software			[SU1] Assessment of task fulfilment		
	[K6_W03] Knows and understands, to an advanced extent, the construction and operating principles of components and systems related to the field of study, including theories, methods and complex relationships between them and selected specific issues - appropriate for the curriculum	Students will demonstrate knowledge of operationing memory addressing rules, program assembling technique, role of interrupts and collaboration CPU with external devices; Students will demonstrate knowledge of microprocessor architecture features, faunctions and applications.			[SW1] Assessment of factual knowledge		

Subject contents	<p>1. Introduction, rules of credit for a course, bibliography 2. The von Neumann computer model, machine and assembler languages 3. Evolution of computer hardware and software, Intel and AMD 32/64 architecture 4. Processor modes (kernel mode, user mode) 5. Main memory 6. Physical information structures 7. General purpose register, control and status register 8. Instruction fetch and execute, instruction cycle 9. Instruction for modifying the flow of control 10. Programming principles at processor instruction level, typical instruction operations 11. Direct and indirect addressing modes 12. Elements of assembly programming: instruction mnemonics, source code formats, variables and labels, directives, Intel and AT&T assembler syntax 13. Macroprocessing 14. Program assembly technique, location counter, one- and two-pass assembly; assembly listing file 15. Stack organization 16. Unconditional branch instruction, procedure call and procedure return 17. Parameters passing to subroutines 18. Passing parameters using stack with hardware support, stack frame 19. Static and local variables access 20. Mixed programming, ABI interface, calling convention (Pascal, C, StdCall) 21. System subroutines, API interface, interrupt descriptor table in IA32 architecture 22. MS Windows and Linux programming interface 23. Computer initialization, BIOS system, BIOS service subroutines 24. Principles of instruction coding formats 25. Base formats in IA 32 architecture 26. Coding of control flow instructions 27. Data formats, signed and unsigned integers, BCD 28. Text coding: ASCII, MS Windows code, ISO codes, Uni-code 29. Arithmetic operations, overflow identification 30. Multiple-precision arithmetic 31. Comparison technique, branch instruction 32. Bit operation, shift and rotate operation 33. Loop instruction, string instructions 34. Fundamental concepts in the control of peripherals 35. Memory mapped input/output control and ports 36. Display memory in the text and graphic mode 37. Serial and parallel communication examples 38. Hardware interrupts, interrupt handler, interrupt priority, masked and unmasked interrupts 39. Hardware interrupt service techniques, IRQ lines mapping on to interrupt vector table 40. System clock service, real time clock 41. Processor exceptions, hardware and software interrupts 42. DMA data transfer 43. Floating point number formats (IEEE 754 standard) 44. Arithmetic floating-point unit as a stack processor, examples of calculations 45. Coprocessor status and control register 46. Exceptions (inexact result, underflow, overflow, not a number) 47. Memory hierarchy: registers, cache memory, main memory, mass memory 48. Memory comparisons 49. Virtual memory as a composite of disk storage and RAM memory 50. Virtual memory with paging, hardware address transformation in Intel/AMD architecture 51. Address transformation support with associative memory 52. Cache memories for data and instructions 53. Cache memory access algorithms 54. Pipeline processing, control collision, branch prediction 55. CISC vs RISC computers 56. Temporal and simultaneous multithreading 57. Multithread and multicore architectures 58. Amdahl's law – computer system scalability 59. Trends in modern computer architecture</p>														
Prerequisites and co-requisites	No requirements														
Assessment methods and criteria	<table border="1"> <thead> <tr> <th>Subject passing criteria</th> <th>Passing threshold</th> <th>Percentage of the final grade</th> </tr> </thead> <tbody> <tr> <td>Practice</td> <td>32.0%</td> <td>25.0%</td> </tr> <tr> <td>Exam</td> <td>10.0%</td> <td>50.0%</td> </tr> <tr> <td>Lab</td> <td>76.0%</td> <td>25.0%</td> </tr> </tbody> </table>			Subject passing criteria	Passing threshold	Percentage of the final grade	Practice	32.0%	25.0%	Exam	10.0%	50.0%	Lab	76.0%	25.0%
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Example issues/ example questions/ tasks being completed															
Work placement	Not applicable														