GDAŃSK UNIVERSITY OF TECHNOLOGY

Subject card

Subject name and code	Hardware Description Languages, PG_00048085		
Field of study	Electronics and Telecommunications		
Date of commencement of studies	October 2021	Academic year of realisation of subject	2023/2024
Education level	first-cycle studies	Subject group	Optional subject group Subject group related to scientific research in the field of study
Mode of study	Full-time studies	Mode of delivery	at the university
Year of study	3	Language of instruction	Polish
Semester of study	6	ECTS credits	3.0
Learning profile	general academic profile	Assessment form	assessment
Conducting unit	Department of Microelectronic Systems -> Faculty of Electronics, Telecommunications and Informatics		
Name and surname of lecturer (lecturers)	Subject supervisor	dr hab. inż. Marek Wójcikowski	
	Teachers	dr hab. inż. Marek Wójcikowski dr hab. inż. Adrian Bekasiewicz dr hab. inż. Waldemar Jendernalik	

Lesson types and methods of instruction	Lesson type	Lecture	Tutorial	Laboratory	Project	Seminar	SUM
	Number of study hours	15.0	0.0	30.0	0.0	0.0	45
	E-learning hours included: 0.0						

Learning activity and number of study hours	Learning activity	Participation in didactic classes included in study plan	Participation in consultation hours	Self-study	SUM
	Number of study hours	45	3.0	27.0	75

Subject objectives	Become acquainted with methods of design and simulations of digital programmable circuits and ASICs using hardware description languages.

Learning outcomes

Course outcome	Subject outcome	Method of verification
[K6_U03] can design, according to required specifications, and make a simple device, facility, system or carry out a process, specific to the field of study, using suitable methods, techniques, tools and materials, following engineering standards and norms, applying technologies specific to the field of study and experience gained in the professional engineering environment	designs digital circuits using the hardware description language;	[SU1] Assessment of task fulfilment [SU3] Assessment of ability to use knowledge gained from the subject [SU4] Assessment of ability to use methods and tools
[K6_W32] Knows the parameters, functions and methods of analysis, design and optimization of analogue and digital circuits and electronic systems	knows specialized software for simulation of electronic circuits, knows methods of manufacturing, scaling and design limitations of integrated circuits, as well as development directions;	[SW1] Assessment of factual knowledge
[K6_U04] can apply knowledge of programming methods and techniques as well as select and apply appropriate programming methods and tools in computer software development or programming devices or controllers using microprocessors or programmable elements or systems specific to the field of study	designs, simulates and debugs programmable digital circuits, implements digital circuits performing typical functions such as time measuring and serial communication;	[SU1] Assessment of task fulfilment [SU3] Assessment of ability to use knowledge gained from the subject [SU4] Assessment of ability to use methods and tools
[K6_W33] Knows programming languages and equipment description languages, as well as methods for the synthesis of combinational and sequential circuits and programmable systems	knows the syntax of hardware design languages and the principles of synthesis and simulation of combinatorial and sequential programmable circuits programming;	[SW1] Assessment of factual knowledge

Subject contents

1. Introduction to and applications of HDL languages. Genesis of Verilog language. 2. Abstraction levels (Verilog). 3. Design methodologies. Simple example. 4. Syntax of Verilog. 5. Data types. 6. System tasks and compilers directives. 7. Modules and ports. 8. Modelling at gate level. 9. Delays in gates. 10. Modelling at register level. 11. Concurrent assignment. 12. Expressions and operators. 13. Modeling at behavioral level. 14. Functions and tasks. 15. Modelling techniques. 16. Verilog 2001 changes in the standard. 17. Genesis of VHDL language. 18. Syntax and data types. 19. Entities and their architectures. 20. Instantiation of components. 21. Concurrent assignments, simple and conditional. 22. Delays, concurrent and time operations. 23. Processes. 24. Conditional commands and loops. 25. Delays with wait keyword. 26. Functions and procedures. 27. Libraries and packages. 28. IEEE library. 29. Synthesis of state machines. 30. Testing the design. 31. Other HDL languages.

Prerequisites and co-requisites

Knowledge of digital circuit technique.

Assessment methods and criteria

Subject passing criteria	Passing threshold	Percentage of the final grade
attendance to the lectures	0.0%	5.0%
2 tests	50.0%	45.0%
lab excercises	50.0%	50.0%

Recommended reading

Basic literature	K.Skahill, Vhdl for Programmable Logic, Addison-Wesley Publishing Company, 1996. S.Palnitkar, Verilog HDL, SunSoft Press, 1996. M. Zwoliński, Projektowanie układów cyfrowych z wykorzystaniem języka VHDL, W.KiŁ, 2002.
Supplementary literature	No requirements
eResources addresses	Adresy na platformie eNauczanie: Języki projektowania HDL 2023/24 - Moodle ID: 26207 https://enauczanie.pg.edu.pl/moodle/course/view.php?id=26207

Example issues/ example questions/ tasks being completed

Work placement

Not applicable