GDAŃSK UNIVERSITY OF TECHNOLOGY

Subject card

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| Subject name and code | Application of FPGA and CPLD in DSP, PG_00048110 | | |
| Field of study | Electronics and Telecommunications | | |
| Date of commencement of studies | October 2021 | Academic year of realisation of subject | 2024/2025 |
| Education level | first-cycle studies | Subject group | Optional subject group<br>Subject group related to scientific research in the field of study |
| Mode of study | Full-time studies | Mode of delivery | at the university |
| Year of study | 4 | Language of instruction | Polish |
| Semester of study | 7 | ECTS credits | 2.0 |
| Learning profile | general academic profile | Assessment form | assessment |
| Conducting unit | Department of Microelectronic Systems -> Faculty of Electronics, Telecommunications and Informatics | | |
| Name and surname of lecturer (lecturers) | Subject supervisor | dr inż. Miron Kłosowski | |
| | Teachers | dr inż. Miron Kłosowski | |

**Lesson types and methods of instruction**

| Lesson type | Lecture | Tutorial | Laboratory | Project | Seminar | SUM |
|---|---|---|---|---|---|---|
| Number of study hours | 15.0 | 0.0 | 15.0 | 0.0 | 0.0 | 30 |

E-learning hours included: 0.0

**Learning activity and number of study hours**

| Learning activity | Participation in didactic classes included in study plan | Participation in consultation hours | Self-study | SUM |
|---|---|---|---|---|
| Number of study hours | 30 | 2.0 | 18.0 | 50 |

**Subject objectives**

The aim of the course is to provide students with the basic knowledge and skills in the design of hardware digital signal processing systems using FPGA technology and VHDL. As a result, students will be prepared to work in companies producing DSP systems using FPGAs or ASICs and students will be able to participate in specialized software development.

**Learning outcomes**

| Course outcome | Subject outcome | Method of verification |
|---|---|---|
| [K6_U04] can apply knowledge of programming methods and techniques as well as select and apply appropriate programming methods and tools in computer software development or programming devices or controllers using microprocessors or programmable elements or systems specific to the field of study | Student designs and implements digital filters using FPGAs. Student measures the characteristics of the implemented filters. | [SU1] Assessment of task fulfilment |
| [K6_W32] Knows the parameters, functions and methods of analysis, design and optimization of analogue and digital circuits and electronic systems | Student specifies functional blocks of DSP systems. Student describes methods of representing DSP algorithms. Student knows the methods of DFG graph optimization. Student understands the concepts of redundant and distributed arithmetic. Student knows the hardware techniques of digital filters implementation. | [SW1] Assessment of factual knowledge |

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| Subject contents | 1. Hardware implementation of DSP systems - introduction. 2. Hardware implementation of FIR digital filters. 3. Automatic DSP modules generation. 4. Hardware implementation and applications of Cascaded Integrator Comb filters. 5. Hardware implementation of IIR digital filters. 6. Rank order filters, median filters. 7. Hardware implementation of DCT and FFT algorithms. 8. Architecture and applications of CORDIC module. 9. Hardware implementation of digital signal synthesis. 10. DSP functional blocks in FPGA circuits architecture and properties. 11. Sample applications of DSP systems based on FPGAs. 12. Description methods of DSP systems. 13. Basic properties of Data Flow Graphs. 14. Iteration bound calculation of DFG using LPM method. 15. Pipeline processing on FIR filter example. 16. Parallel processing on FIR filter example. 17. Power efficiency of pipeline and parallel processing. 18. Retiming. Retiming algorithms. K-slow transform. 19. Unfolding - properties and applications. 20. Folding - properties and applications. 21. Systolic arrays. 22. Canonic Signed Digit arithmetics. 23. Distributed arithmetic. 24. Redundant arithmetic. 25. Numerical strength reduction. |
| Prerequisites and co-requisites | |
| Assessment methods and criteria | |

| Subject passing criteria | Passing threshold | Percentage of the final grade |
|---|---|---|
| Midterm colloquium | 50.0% | 50.0% |
| Practical exercise | 50.0% | 50.0% |

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| Recommended reading | Basic literature | 1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems - Design and Implementation", John Wiley and Sons, Inc; 1999.<br>2. Tomasz P. Zieliński, "Cyfrowe przetwarzanie sygnałów - od teorii do zastosowań", Wydawnictwa Komunikacji i Łączności, Warszawa 2005. |
| | Supplementary literature | No requirements |
| | eResources addresses | Adresy na platformie eNauczanie:<br>Zastosowanie FPGA i CPLD w systemach CPS 2024/25 - Moodle ID: 38528<br>https://enauczanie.pg.edu.pl/moodle/course/view.php?id=38528 |
| Example issues/ example questions/ tasks being completed | Design using any method low-pass FIR filter with provided parameters and implement it on the laboratory evaluation board. | |
| Work placement | Not applicable | |

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