

。 GDAŃSK UNIVERSITY OF TECHNOLOGY

Subject card

Subject name and code	Design of ASIC, PG_00048109							
Field of study	Electronics and Telecommunications							
Date of commencement of studies	October 2022		Academic year of realisation of subject			2025/2026		
Education level	first-cycle studies		Subject group			Optional subject group Subject group related to scientific research in the field of study		
Mode of study	Full-time studies		Mode of delivery			at the university		
Year of study	4		Language of instruction			Polish		
Semester of study	7		ECTS credits		4.0			
Learning profile	general academic profile		Assessme	Assessment form		exam		
Conducting unit	Department of Microelectronic Systems -> Faculty of Electronics, Telecommunications and Informatics							
Name and surname of lecturer (lecturers)	Subject supervisor		dr hab. inż. Bogdan Pankiewicz					
	Teachers		dr hab. inż. Bogdan Pankiewicz					
Lesson types and methods	Lesson type	Lecture	Tutorial	Laboratory	Projec	t	Seminar	SUM
of instruction	Number of study hours	15.0	0.0	15.0	15.0		0.0	45
	E-learning hours included: 0.0							
Learning activity and number of study hours	Learning activity	Participation in didactic classes included in study plan		Participation in consultation hours		Self-study		SUM
	Number of study hours	45		4.0		51.0		100
Subject objectives	knows programmable integrated microelectronic systems, can design digital integrated circuit using standard cells approach and specialized design tools							

IP6_W33 (down programmable description languages and explained description languages) and explained of the description languages and explained and the description languages and explained and the description language the description languages and explained and the description of the tadge of distance and the description of the description of the tadge of distance and the description of the tadge of distance and the description of the description of the tadge of distance and the description of the description of the tadge of distance and the description of the description of the description of the tadge of distance and the description of the description of the description of the description	Learning outcomes	Course outcome	Subject outcome	Method of verification				
Subject contents In characterized and segments of analysis. Integrated AC and CA converters. basic digital cruits, output and input biffer blocks. Invokedge If KE_UDB can analyse the operation of components, orcinits study, measure their parameters and examine technical specifications Student is able to estimate the opsatile rotic cruits and study measure their parameters and examine technical specifications Student is able to estimate the opsatile rotic cruits as the components, and spin technical specifications Student is able to estimate the opsatile rotic cruits as the components and spin technical possible rotic cruits and technology she and advanced technology and and spin technology of ASICs, explains the problems associated with the design of ASICs, explains the problems associated with the design of ASICs and explains the problems associated and complex software develops and complex provide programming selected splace contents [SU1] Assessment of task fulfilment Subject contents 1.1 C technologies, technological steps, design nules, IC devices and its drawbacks. 2. Relative and absolute mismatch and devices design for matching in-provement. 3. Classification and general information regarding integrated digital doracits. Review o		languages and equipment description languages, as well as methods for the synthesis of combinational and sequential circuits and programmable	techniques (Design For Test). Student knows the methods of testing digital and analog circuits. Student knows the basic properties and principles of using serial interfaces used for integrated circuits and PCB assembly testing, including an interface in accordance with the	[SW1] Assessment of factual				
Subject contents 1. IC technologies, technological steps, design rules, IC devices and its drawbacks. 2. Relative and absolute integrated circuit, respective to a study. [SUBJect contents Subject contents 1. IC technologies, technological steps, design rules, IC devices and its drawbacks. 2. Relative and absolute integrated provided and device design of galax 9. Goods [SUBJect contents Subject contents 1. IC technologies, technological steps, design rules, IC devices and its drawbacks. 2. Relative and absolute integrated of concenters in the standard galaxies of concenters in the standard galaxies of concenters. [SUBJect contents Subject contents 1. IC technologies, technological steps, design rules, IC devices and its drawbacks. 2. Relative and absolute integrated direct with the standard galaxies of concenters. Is the standard galaxies of concenters. Subject contents 1. IC technologies, technological steps, design rules, IC devices and its drawbacks. 2. Relative and absolute mismatch and devices design from tacting importenters. Is the standard galaxies of concenters. Subject contents 1. IC technologies, technological steps, design rules, IC devices and its drawbacks. 2. Relative and absolute programming methods and optimal free free of study. Recommended reading 1. IC technologies, technological steps. design rules, IC devices and its drawbacks. 2. Relative and absolute programming regrammative information regarding integrated digital to analog converters. 4. IC realization of steps of AC converters. 5. Classification and general information regarding integrated digital to		functions and methods of analysis, design and optimization of analogue and digital circuits and	integrated AC and CA converters, basic digital circuits, output and					
stant, the construction and operating principles of complex spectrate with the design of ASICs and explains the methods for eliminating parasitics. incoviédge internet stant systems related to the field of study, including theories, methods and complex relationships between them and selected specific issues - appropriate for the curriculum internet specific issues - appropriate for the curriculum [SU1] Assessment of task fulfilment INF_UCID_(Can apply knowledge of programming methods and techniques as well as select and apply appropriate programming devices or controllers using microprocessors or systems specific to the field of study Student is able to design a digital integrated circuit using HDL perform a description of the description, perform logical synthesis and implementation in the standard circuits and devices eign for matching improvement - assituation of the description, perform logical synthesis and implementation in the standard circuits and devices design for matching improvement - 3. Classification and general information regarding integrated digital to change and the description of selected DA converters. 5. Classification and general information or apparent or programming integrated digital is change and the bit of class and the description of the tectoral curve of commercial EDA tools (Cadence). 11. Testability of ASICs. Design of 10 for testability 12. Interface IEEE 1149.1. 13. Application of files. 8. Class three 10. Classification and general information or propagation times and optical sectoral systems. 15. Future of ASICs and ICs. Subject contents Subject passing criteria Passing threshold Percentage of the final grade Project 51.0% 25.0% Cassification of		operation of components, circuits and systems related to the field of study, measure their parameters and examine technical	delays of basic logic circuits as well as input-output blocks. Student is able to estimate the possible resolutions of AC and CA converters realized in CMOS					
Integrated circuit using HDL inquigues, Student is able to apply appropriate programming methods and tools in computer software development or programming devices or controllers using microprocessor or programmable elements or systems specific to the field of study Integrated circuit, then perform a simulation of the description, perform logical synthesis and cells techniques. Infiliment Subject contents 1. IC technologies, technological steps, design rules, IC devices and its drawbacks, 2. Relative and absolute mismentation in the standard cells techniques. 1. IC technologies, technological steps, design rules, IC devices and its drawbacks, 2. Relative and absolute mismentation and general information regarding integrated analog to organization of selected DA converters, 5. Classification and general information regarding integrated analog to digital circuits and IC realization of selected DA converters, 5. Classification and general information regarding integrated analog to digital circuits and IC realization of selected DA converters, 5. Subple and hold circuits and IC realization of selected DA converters, 5. Subple and hold circuits and IC realization of selected DA converters, 5. Subple and hold circuits and IC automated design of digital circuits. Review of commercial EDA tools (Cadence), 11. Testability of ASICs. Design of IC for testability, 12. Interface IEEE 1149, 1.13. Application of interface IEE 1149, 1.10 Automated design of VHDL or Verilog. Assessment methods and criteria Subject passing criteria Passing threshold Percentage of the final grade Project Froject 51.0% 25.0% Weittere, EEE Journal of Solod-State Circuits, vol. 24, no. 5. October 1999, K. P. Parker, The Boundary-Scane H		understands, to an advanced extent, the construction and operating principles of components and systems related to the field of study, including theories, methods and complex relationships between them and selected specific issues -	technology of ASICs, explains the problems associated with the design of ASICs and explains the					
bitsport softened mismatch and devices design for matching in-provement. 3. Classification and general information regarding integrated digital to analog converters. 4. IC realization of selected DA converters. 5. Classification and general information regarding integrated analog to digital converters. 6. Sample and hold circuits and IC realization of selected DA converters. 7. General digital cells: gates and flip flops. 8. Estimation of propagation times and optimal design of gates. 9. Clock tree topologies and synthesis of clock tree. 10. Automated design of lice. 14. Design of mixed circuits and systems. 15. Future of ASICs and ICs. Prerequisites Knowledge of VHDL or Verilog. and correquisites Knowledge of VHDL or Verilog. Assessment methods Subject passing criteria Passing threshold Percentage of the final grade Project 51.0% 25.0% Recommended reading Basic literature Matching properties of MOS transistors, M. Pelgrom, A. Duinmaijer, A. Welbres, IEEE Journal of Solid-State Circuits, vol. 24, no. 5, October 1989. K. P. Parker, The Boundary-Scan Handbook Second Edition Analog and Digital, Kluwer Academic Publishers, 1998. C. Wai-Kai (editor), The VLSI Handbook, Taylor & Francis Group, 2007. Supplementary literature No requirements eResources addresses Adresy na platformie eNauczanie:		programming methods and techniques as well as select and apply appropriate programming methods and tools in computer software development or programming devices or controllers using microprocessors or programmable elements or systems specific to the field of	integrated circuit using HDL languages. Student is able to perform a description of the integrated circuit, then perform a simulation of the description, perform logical synthesis and implementation in the standard					
Prerequisites Knowledge of VHDL or Verilog. Assessment methods and criteria Subject passing criteria Passing threshold Percentage of the final grade Project 51.0% 25.0% Written exam 51.0% 50.0% Practical exercise 51.0% 25.0% Recommended reading Basic literature Matching properties of MOS transistors, M. Pelgrom, A. Duinmaijer, A. Welbres, IEEE Journal of Solid-State Circuits, vol 24, no. 5, October 1989, K. P. Parker, The Boundary-Scan Handbook Second Edition Analog and Digital, Kluwer Academic Publishers, 1998. C. Wai-Kai (editor), The VLSI Handbook, Taylor & Francis Group, 2007. Supplementary literature No requirements eResources addresses Adresy na platformie eNauczanie:	Subject contents	mismatch and devices design for matching im-provement. 3. Classification and general information regarding integrated digital to analog converters. 4. IC realization of selected DA converters. 5. Classification and general information regarding integrated analog to digital converters. 6. Sample and hold circuits and IC realization of selected DA converters. 7. General digital cells: gates and flip flops. 8. Estimation of propagation times and optimal design of gates. 9. Clock tree topologies and synthesis of clock tree. 10. Automated design of digital circuits. Review of commercial EDA tools (Cadence). 11. Testability of ASICs. Design of IC for testability. 12. Interface IEEE 1149.1. 13. Application of interface IEE1149.1 for testing of						
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Work placement Not applicable	example questions/							
	Work placement	Not applicable						

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