

Subject card

Subject name and code	Analog Integrated Circuits, PG_00048108								
Field of study	Electronics and Telecommunications								
Date of commencement of studies	October 2022		Academic year of realisation of subject			2025/2026			
Education level	first-cycle studies		Subject group			Optional subject group Subject group related to scientific research in the field of study			
Mode of study	Full-time studies		Mode of delivery			at the university			
Year of study	4		Language of instruction			Polish			
Semester of study	7		ECTS credits			2.0			
Learning profile	general academic profile		Assessment form			assessment			
Conducting unit	Department of Microelectronic Systems -> Faculty of Electronics, Telecommunications and Informatics					rmatics			
Name and surname	Subject supervisor	dr hab. inż. Jacek Jakusz							
of lecturer (lecturers)	Teachers		dr hab. inż. Jacek Jakusz						
Lesson types and methods of instruction	Lesson type	Lecture	Tutorial	Laboratory	Projec	ject Seminar		SUM	
	Number of study hours	15.0	0.0	15.0	0.0		0.0	30	
	E-learning hours included: 0.0								
Learning activity and number of study hours	Learning activity Participation in classes include plan				Self-study SUM				
	Number of study hours			2.0		18.0		50	
Subject objectives	The aim of the course is to provide knowledge of design analog integrated circuits and gain practical skills in design and performance verification of analog circuits using CAD software.								
Learning outcomes	Course outcome		Subject outcome			Method of verification			
	[K6_W32] Knows the parameters, functions and methods of analysis, design and optimization of analogue and digital circuits and electronic systems		The student lists and classifies and describes the basic technologies of IC manufacturing. The student recognizes and describes basic functional blocks of analogue integrated circuits. The student recognizes and describes basic circuits: operating amplifiers, transconductance amplifiers and comparators. The student calculates basic parameters of analog amplifying circuits.			[SW3] Assessment of knowledge contained in written work and projects [SW1] Assessment of factual knowledge			
	required specifications, and make a simple device, facility, system or		Student calculates parameters of simple analog circuits. Student designs topographies of simple analog circuits. The student simulates and evaluates parameters of analog circuits.			[SU4] Assessment of ability to use methods and tools [SU1] Assessment of task fulfilment			

Subject contents	1. CMOS, BJT & BiCMOS analog integrated circuits introduction 2. Modeling of CMOS and BJT devices 3. Passive components in analog integrated circuits 4. Basic building blocks: MOS switches, MOS Current Sinks/Sources 5. Basic building blocks: current mirrors, MOS resistors, active loads 6. Basic building blocks: single stage amplifiers 7. Basic building blocks: output amplifiers/buffers 8. Voltage and current reference circuits 9. Operational amplifiers - design principles and compensation 10. Architecture of two-stage CMOS operational amplifier 11. Design procedure of two-stage CMOS operational amplifier 12. High-performance CMOS operational amplifiers - examples 13. Operational transconductance amplifiers OTA linearization methods 14. OTA realization - examples 15. Current conveyors and current amplifiers 16. CMOS comparators						
Prerequisites and co-requisites	No requirements						
Assessment methods and criteria	Subject passing criteria	Passing threshold	Percentage of the final grade				
	Midterm colloquium	50.0%	60.0%				
	Practical exercise	50.0%	40.0%				
Recommended reading	Basic literature	D. Johns, K. Martin: Analog Integrated Circuit Design, John Wiley & Sons, Inc. P.E. Allen, D.R. Holberg: CMOS Analog Circuit Design, Oxford University Press Jacek Izydorczyk: Pspice. Komputerowa symulacja układów elektronicznych, Helion					
	Supplementary literature	No requirements	No requirements				
	eResources addresses	Adresy na platformie eNauczanie:					
Example issues/ example questions/ tasks being completed	Design of a two-stage CMOS operational amplifier.						
Work placement	Not applicable						

Document generated electronically. Does not require a seal or signature.

Data wygenerowania: 14.04.2025 22:29 Strona 2 z 2