GDAŃSK UNIVERSITY OF TECHNOLOGY

Subject card

Subject name and code	Design of VLSI Circuits, PG_00048579		
Field of study	Electronics and Telecommunications		
Date of commencement of studies	February 2023	Academic year of realisation of subject	2022/2023
Education level	second-cycle studies	Subject group	Optional subject group Subject group related to scientific research in the field of study
Mode of study	Full-time studies	Mode of delivery	at the university
Year of study	1	Language of instruction	English
Semester of study	1	ECTS credits	1.0
Learning profile	general academic profile	Assessment form	assessment
Conducting unit	Department of Microelectronic Systems -> Faculty of Electronics, Telecommunications and Informatics		
Name and surname of lecturer (lecturers)	Subject supervisor	dr hab. inż. Adrian Bekasiewicz	
	Teachers	dr hab. inż. Adrian Bekasiewicz	

Lesson types and methods of instruction

Lesson type	Lecture	Tutorial	Laboratory	Project	Seminar	SUM
Number of study hours	15.0	0.0	0.0	0.0	0.0	15

E-learning hours included: 0.0

Learning activity and number of study hours

Learning activity	Participation in didactic classes included in study plan	Participation in consultation hours	Self-study	SUM
Number of study hours	15	2.0	8.0	25

Subject objectives

Introduction to design of VLSI circuits with emphasis on discussion of algorithmic approaches used for generation of their topologies

Learning outcomes

Course outcome	Subject outcome	Method of verification
[K7_W04] Knows and understands, to an advanced extent, the principles, methods and techniques of programming and the principles of computer software development or programming devices or controllers using microprocessors or programmable elements or systems specific to the field of study, and organisation of systems using computers or such devices	The student is acquainted with algorithms utilized in VLSI circuits design (objective functions, working principles, constraints, etc.) and can select appropriate algorithm for solving problems at the given design stage.	[SW3] Assessment of knowledge contained in written work and projects
[K7_U07] can apply advanced methods of process and function support, specific to the field of study	The student can exploit algorithmic approaches for solving tasks resulting from the selected stages of VLSI circuits design	[SU1] Assessment of task fulfilment [SU2] Assessment of ability to analyse information
[K7_W03] Knows and understands, to an increased extent, the construction and operating principles of components and systems related to the field of study, including theories, methods and complex relationships between them and selected specific issues - appropriate for the curriculum.	The student is acquainted with selected topics related to VLSI circuit design, as well as understands basic design steps and their significance from the perspective of topology generation.	[SW3] Assessment of knowledge contained in written work and projects
[K7_K02] is ready to provide critical evaluation of received content and to acknowledge the importance of knowledge in solving cognitive and practical problems	The student can perform analysis of the discussed algorithmic approaches in terms oftheir advantages and disadvantages in the constext of VLSI circuits design.	[SK2] Assessment of progress of work

Subject contents

1. Introduction to VLSI circuits design:
    1. historical perspective,
    2. development of integrated circuits,
    3. challenges and future prospects
2. Design of VLSI circuits:
    1. hierarchical design approach,
    2. photolithography,
    3. rules for layout generation,
    4. design styles,
    5. layout design steps,
    6. packages used for VLSI circuits,
    7. problem complexity
3. Introduction to graph theory
    1. Matrix-based representations of graphs
    2. Hipergraphs
    3. Graph-based approximation of electronic circuits
    4. Selected graph-based algorithms
4. Partitioning
    1. The problem of partitioning at different layers of abstraction
    2. Challenges related to circuit partitioning
    3. Selected partitioning algorithms
5. Floorplanning
    1. The role of floorplanning in hierarchical design process
    2. Problem definition and objective functions
    3. Cluster growth and linear ordering algorithms
    4. Simulated annealing and data representation schemes
    5. Calculation of size
    6. Analytical approach to floorplanning
    7. Floorplanning and routing – discussion
6. Placement
    1. Problem definition, objective functions, and complexity
    2. Solution approaches to placement
    3. Linearization techniques
    4. The problem of modules overlapping and related constraints
    5. Dealing with conflicts – legalization
    6. Detailed placement and related algorithms
7. Routing
    1. Problem definition, constraints, and routing models
    2. Selected routing algorithms (maze, line-search, A*-search)
    3. Global routing – sequential and parallel approaches to the problem
    4. Detailed routing – selected algorithms
    5. Full-chip routing – hierarchical and multi-level approaches
    6. Modern challenges in the context of routing (signal integrity, fabrication, reliability)
8. Synthesis of clock and power networks for VLSI
    1. Review of clock signal networks
    2. Algorithms for generation of clock networks
    3. Design of power networks
    4. Optimization in the context of power networks design
    5. Noise
9. Fault simulation and testing
    1. Significance of testing for mass production
    2. Approaches to VLSI circuits testing in the context of problem complexity
    3. Automatic test pattern generation

Prerequisites and co-requisites

Assessment methods and criteria

Subject passing criteria	Passing threshold	Percentage of the final grade
Assignments	50.0%	40.0%
Final test	50.0%	50.0%
Attendance	0.0%	10.0%

Recommended reading

Basic literature

1. N.A. Sherwani, Algorithms for VLSI physical design automotion, 3rd ed. Kluwer Academic Publishers, Boston, 1999.
2. L.-T. Wang, Y.-W. Chang, and K.-T. Cheng, Electronic design automation: synthesis, verification, and test, The Morgan Kaufmann Series in Systems on Silicon, Amsterdam, 2009.
3. S.M. Sait and H. Youssef, VLSI physical design automation: theory and practice, IEEE Press, New York, 1995.
4. C.H. Papadimitriou, K. Steiglitz, Combinatorial optimization: algorithms and complexity, Dover Publications, Mineola, 1998.
5. M. Sarrafzadeh, C.K. Wong, An introduction to VLSI physical design, Mc-Graw-Hill Series in Computer Science, New York, 1996.
6. A.B. Kahng, J. Lienig, I.L. Markov, and, J. Hu, VLSI Physical Design: From Graph Partitioning to Timing Closure, Springer, 2011.

Supplementary literature

1. R.J. Baker, CMOS: circuit design, layout, and simulation, IEEE Press & Wiley, Hoboken, 2010
2. N.H.E. Weste and D.M. Harris, CMOS VLSI design: a circults and systems perspective, Addison-Wesley, Boston, 2011.
3. W.-K. Chen (Ed.), The VLSI handbook, CRC Press, Boca Raton, 2007.
4. C.J. Alpert, D.P. Mehta, S.S. Sapatnekar (eds.), Handbook of Algorithms for Physical designAutomation, CRC Press, 2009.

eResources addresses

Adresy na platformie eNauczanie:

Example issues/ example questions/ tasks being completed	
Work placement	Not applicable