GDAŃSK UNIVERSITY OF TECHNOLOGY

Subject card

Subject name and code	Integrated Circuits for Computer Networks, PG_00048582
Field of study	Electronics and Telecommunications

Date of commencement of studies	February 2024	Academic year of realisation of subject	2024/2025
Education level	second-cycle studies	Subject group	Optional subject group Subject group related to scientific research in the field of study
Mode of study	Full-time studies	Mode of delivery	at the university
Year of study	1	Language of instruction	Polish
Semester of study	2	ECTS credits	3.0
Learning profile	general academic profile	Assessment form	exam

Conducting unit	Department of Microelectronic Systems -> Faculty of Electronics, Telecommunications and Informatics

Name and surname of lecturer (lecturers)	Subject supervisor	dr inż. Miron Kłosowski
	Teachers	dr inż. Miron Kłosowski

Lesson types and methods of instruction	Lesson type	Lecture	Tutorial	Laboratory	Project	Seminar	SUM
	Number of study hours	15.0	0.0	30.0	0.0	0.0	45
	E-learning hours included: 0.0						

Learning activity and number of study hours	Learning activity	Participation in didactic classes included in study plan	Participation in consultation hours	Self-study	SUM
	Number of study hours	45	6.0	24.0	75

Subject objectives	The aim of the course is to develop a specialist having advanced knowledge and skills in the design, verification and testing of digital systems for computer networks, built using FPGAs and network processors. Graduates are prepared to work in companies producing equipment that uses computer networks. They are also prepared to participate in research programs where networking devices are developed or used.

Learning outcomes	Course outcome	Subject outcome	Method of verification
	[K7_U04] can apply knowledge of programming methods and techniques as well as select and apply appropriate programming methods and tools in computer software development or programming devices or controllers using microprocessors or programmable elements or systems specific to the field of study, making assessment and critical analysis of the prepared software as well as a synthesis and creative interpretation of information presented with it	Student applies FPGA ICs for the implementation of algorithms related to computer networks and communication with integrated circuits providing support for selected layers of the ISO/OSI model.	[SU1] Assessment of task fulfilment
	[K7_W04] Knows and understands, to an advanced extent, the principles, methods and techniques of programming and the principles of computer software development or programming devices or controllers using microprocessors or programmable elements or systems specific to the field of study, and organisation of systems using computers or such devices	Student knows and understands the algorithms of computer networks and their hardware implementation, structure and properties of network processors, switches, routers, interfaces and integrated circuits providing support for selected layers of the ISO/OSI model.	[SW1] Assessment of factual knowledge

Subject contents	1. Evolution of microprocessors and computer networks. 2. Network processors - introduction. 3. Architecture of IXP network processor family. 4. Internal structure of the microengine. 5. Memories and addressing modes in the microengine. 6. Multithreading in microengine. 7. Communication between microengines. 8. Function modules in the microengine. 9. Function modules of IXP network processor. 10. M-packet communication service. 11. Introduction to assembler language of IXP family network processors. 12. C language in network processor programming. 13. Packet processing by unordered thread execution. 14. Packet processing by context pipeline stages. 15. Packet processing by ordered thread execution. 16. Data structure support in IXP processors - rings and queues. 17. Applications of network processors in switches, routers and firewalls. 18. Standards of computer networks and cabling. 19. PHY layer. Auto-negotiation procedures. 20. MAC layer. Addressing methods. 21. Programmable ICs for medium attachment. 22. Media Independent Interface - description of the standard. 23. Frame sending and receiving by MII. 24. "Full duplex" mode and flow control mechanizms. 25. Multicast addressing implementation. 26. Programmable ICs for frame assembly/disassembly. 27. VLAN networks and their implementation. 28. Port aggregation mechanisms. 29. Memories for computer network systems. 30. CAM and TCAM memories. 31. One-dimensional classifiers. 32. Multi-dimensional classifiers. 33. Switch architecture. Algorithms and processes. 34. Router architecture. Algorithms and processes. 35. Hardware acceleration of "Quality of Service" mechanisms. 36. Hardware acceleration of layers 4-7. 37. Cryptographic coprocessors. 38. ICs for wireless networks.

Prerequisites and co-requisites	

Assessment methods and criteria			
	Subject passing criteria	Passing threshold	Percentage of the final grade
	Practical exercise	50.0%	70.0%
	Written exam	50.0%	30.0%

Recommended reading	Basic literature	1. Erik J. Johnson, Aaron R. Kunze, "IXP2400/2800 Programming", Intel Press 2003. 2. George Varghese, "Network Algorithmics", Elsevier/ Morgan Kaufmann, 2005. 3. Rich Seifert, "The Switch Book", John Wiley & Sons, 2000.
	Supplementary literature	No requirements
	eResources addresses	Adresy na platformie eNauczanie:

Example issues/ example questions/ tasks being completed	

Work placement	Not applicable