GDAŃSK UNIVERSITY OF TECHNOLOGY

Subject card

Subject name and code	Programmable Systems Engineering, PG_00047897		
Field of study	Informatics		
Date of commencement of studies	October 2024	Academic year of realisation of subject	2026/2027
Education level	first-cycle studies	Subject group	Optional subject group Subject group related to scientific research in the field of study
Mode of study	Full-time studies	Mode of delivery	at the university
Year of study	3	Language of instruction	Polish
Semester of study	6	ECTS credits	4.0
Learning profile	general academic profile	Assessment form	assessment
Conducting unit	Department of Microelectronic Systems -> Faculty of Electronics, Telecommunications and Informatics		
Name and surname of lecturer (lecturers)	Subject supervisor	dr inż. Miron Kłosowski	
	Teachers	dr inż. Miron Kłosowski	

Lesson types and methods of instruction	Lesson type	Lecture	Tutorial	Laboratory	Project	Seminar	SUM
	Number of study hours	15.0	0.0	30.0	0.0	0.0	45
	E-learning hours included: 0.0						

Learning activity and number of study hours	Learning activity	Participation in didactic classes included in study plan	Participation in consultation hours	Self-study	SUM
	Number of study hours	45	2.0	53.0	100

Subject objectives	The aim of the course is to provide students with the basic knowledge and skills in the design of digital electronic systems using FPGA technology and VHDL. As a result, students will be prepared to work in companies producing electronic systems using FPGAs and students will be able to participate in specialized EDA software development.

Learning outcomes

Course outcome	Subject outcome	Method of verification
[K6_W10] knows and understands to an advanced degree the basic processes occurring in the life cycle of equipment, objects and technical systems, as well as methods of supporting processes and functions, specific to the field of study	Student describes techniques for supporting the design of complex logic circuits and describes hardware techniques of algorithm acceleration.	[SW1] Assessment of factual knowledge
[K6_W03] knows and understands, to an advanced extent, the construction and operating principles of components and systems related to the field of study, including theories, methods and complex relationships between them and selected specific issues - appropriate for the curriculum	Student describes the architecture and applications of SPLD and FPGA digital programmable circuits. Student describes FPGA configuration methods.	[SW1] Assessment of factual knowledge
[K6_W04] knows and understands, to an advanced extent, the principles, methods and techniques of programming and the principles of computer software development or programming devices or controllers using microprocessors or programmable elements or systems specific to the field of study, and organisation of systems using computers or such devices	Student describes the properties of hardware description languages. Student knows the basics of the VHDL hardware description language. Student understands the processes of synthesis and simulation. Student is able to determine the conditions for the synthesis of the code in VHDL. Student knows the basics of the SystemC environment.	[SW1] Assessment of factual knowledge
[K6_U03] can design, according to required specifications, and make a simple device, facility, system or carry out a process, specific to the field of study, using suitable methods, techniques, tools and materials, following engineering standards and norms, applying technologies specific to the field of study and experience gained in the professional engineering environment	Student designs digital circuits using VHDL and SystemC hardware description languages. Student simulates the behavior of designed systems using VHDL and SystemC simulators. Student implements and tests digital systems in a real hardware-software environment based on FPGAs.	[SU1] Assessment of task fulfilment

Subject contents

1. Introduction to VHDL, origin and applications. 2. Abstraction levels and description methods of digital circuits. 3. Design entity description in VHDL. 4. Assignments, signals, variables and operators in VHDL. 5. Data types in VHDL. 6. Resolution function. 7. Vectors and operations on vectors in VHDL. 8. Combinatorial processes. Synthesis of combinatorial logic in VHDL. 9. Project simulation in VHDL. 10. Conditional, case and loop statements in processes. 11. Constants and initial values of signals and variables. 12. Hierarchy and configuration of design entities. 13. Sequential processes in VHDL. 14. State machines. State encoding. Forbidden states. 15. Type conversion in VHDL. 16. Functions and procedures in VHDL. 17. Introduction to SystemC environment. 18. Applications of SystemC environment. 19. System design with hardware-software partitioning. 20. System on Chip technology. 21. Soft-processors - architecture and applications. 22. Programmable circuits taxonomy. 23. Architecture of FPGAs. 24. Configuration methods of FPGAs. 25. Hardware functional blocks in FPGAs. 26. "Reconfigurable computing" as a programming paradigm. 27. Applications of RC in signal processing. 28. Applications of RC in image processing. 29. Applications of RC in teleinformatics. 30. Applications of RC in supercomputers. 31. Algorithm representation in RC. 32. Arithmetic systems in RC. 33. "Network on Chip" technology.

Prerequisites and co-requisites

Assessment methods and criteria

Subject passing criteria	Passing threshold	Percentage of the final grade
Midterm colloquium	50.0%	30.0%
Practical exercise	50.0%	70.0%

Recommended reading

Basic literature	Zwoliński Mark, "Projektowanie układów cyfrowych z wykorzystaniem języka VHDL", Wydawnictwa Komunikacji i Łączności WKŁ, Warszawa 2007.
Supplementary literature	No requirements
eResources addresses	Adresy na platformie eNauczanie:

Example issues/ example questions/ tasks being completed	Sample lab exercises: 1. Simple LED display driver. 2. Simple RS232 receiver and transmitter. 3. Video signal generator for VGA display. 4. Embedded system based on FPGA.
Work placement	Not applicable

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