GDAŃSK UNIVERSITY OF TECHNOLOGY

Subject card

Subject name and code	Digital Technology I, PG_00047528		
Field of study	Automatic Control, Cybernetics and Robotics		
Date of commencement of studies	October 2024	Academic year of realisation of subject	2024/2025
Education level	first-cycle studies	Subject group	Obligatory subject group in the field of study
Mode of study	Full-time studies	Mode of delivery	at the university
Year of study	1	Language of instruction	Polish
Semester of study	1	ECTS credits	7.0
Learning profile	general academic profile	Assessment form	exam
Conducting unit	Department of Automatic Control -> Faculty of Electronics, Telecommunications and Informatics		
Name and surname of lecturer (lecturers)	Subject supervisor	dr inż. Paweł Raczyński	
	Teachers	dr inż. Marcin Pazio dr inż. Kamil Stawiarski dr inż. Sebastian Dziedziewicz dr inż. Paweł Raczyński	

Lesson types and methods of instruction

Lesson type	Lecture	Tutorial	Laboratory	Project	Seminar	SUM
Number of study hours	30.0	30.0	0.0	0.0	0.0	60
E-learning hours included: 0.0						

Learning activity and number of study hours

Learning activity	Participation in didactic classes included in study plan	Participation in consultation hours	Self-study	SUM
Number of study hours	60	7.0	108.0	175

Subject objectives

The aim of the course is to learn the mathematical description and the methods of analysis and design of digital integrated curcuits

Learning outcomes

Course outcome	Subject outcome	Method of verification
[K6_W03] knows and understands, to an advanced extent, the construction and operating principles of components and systems related to the field of study, including theories, methods and complex relationships between them and selected specific issues - appropriate for the curriculum	He knows and understands the methods of description of digital circuits. He knows the techniques of design and optimization of combinational and sequential digital circuits. He knows the components of digital circuits, knows the technologies of their production and the rules for combining them.	[SW1] Assessment of factual knowledge
[K6_U03] can design, according to required specifications, and make a simple device, facility, system or carry out a process, specific to the field of study, using suitable methods, techniques, tools and materials, following engineering standards and norms, applying technologies specific to the field of study and experience gained in the professional engineering environment	339/5000 Is able to independently analyze the combined and sequential digital system. He can go from his scheme to the formal description. Is able to independently design a combination or sequential digital circuit in the optimal version. He can make the technical implementation of the designed system taking into account different technologies.	[SU4] Assessment of ability to use methods and tools [SU2] Assessment of ability to analyse information [SU1] Assessment of task fulfilment

Subject contents	1. Basic definition and notions: combinational and sequential circuits (CCs and SCs). 2. Description of CCs: logic functions and truth tables, description of SCs: state transition tables and diagrams for Moore and Mealy models. Examples of CCs and SCs circuits. 3. Positional number systems: decimal, binary, octal, hexadecimal. 4. Signed number representation U1, U2, and binary arithmetic, floating-point notation. 5. Postulates and fundamental theorems of Boolean Algebra. 6. Important logic functions, functionally complete systems, canonical forms of logic functions – some practical transfor-mations. 7. SOP and POS forms, other Algebras examples, exemplary uses of Boolean Algebra – connecting networks 8. Simplification of logic functions, usage of Boolean Algebra theorems, simplification aims: economical and technical. 9. Simplification of logic functions using Karnaugh maps. 10. Simplification of logic functions: implicants and implicates, Quine-McCluskey methode, examples of simplification. 11. Basic logic gates, CC design with logic gates AND, OR, NOT. 12. CC design with logic gates NAND and NOR. Some remarks on simplification of SOP and POS forms contrary global simplification, transition times. 13. Look through standard CC circuits. 14. Multiplexers / demultiplexers and their use in designing CCs, multiplexer and logical gates mixed techniques design-ing. 15. Iterative CCs: the concept and basic variants, system complexity response time compromise. 16. Abstract synthesis of synchronous sequential circuits (SSCs). Constructing of state diagram and the need for state re-duction, state reduction procedure 17. State coding, flip-flops – input tables and triggering, examples. 18. Combinational synthesis of SSCs, design examples. 19. SSCs analysis, conversion between Moore and Mealy models. 20. Synthesis of asynchronous sequential circuits (ASCs), new aspects in abstract synthesis 21. Signal timings and the concept of state, constructing of state diagram for an ASC, races and race-free coding, 22. Types of asynchronous circuits, unclocked memory elements, synthesis of a feedback-type ASC, synthesis of an ASC with SR-latches. 23. Combinational synthesis of ASCs, using Karnaugh-maps to eliminate timing hazards, design examples. 24. Technical aspects of digital circuits design, TTL and CMOC technologies, some SSI and LSI components. 25. Digital circuits: parameters and characteristics in bipolar and complementary MOS technologies, circuit families and component compatibilities. 26. Technical aspects of digital circuits design, OC and TS gates, bus organization techniques. Different circuits family's member interconnections. 27. Standard MSI components – synchronous and asynchronous counters, and their applications. 28. Standard MSI components – synchronous and asynchronous registers, and their applications; bus organization – ad-dressing techniques and timings. 29. Selected digital circuits: monostable and astable flip-flops, read-only memories (ROM, PROM, EPROM, EEPROM), parameters, timings and usage for CCs design. 30. Selected digital circuits: dynamic and static read-write memories, introducing into programmable logic (PLA), CCs design using PLA.
Prerequisites and co-requisites	No requirements
Assessment methods and criteria	

Subject passing criteria	Passing threshold	Percentage of the final grade
2 classworks for 20 points each, test for 30 point, possibitity to correct score with any subset of items at exam session	51.0%	60.0%
open test examination	51.0%	40.0%

Recommended reading	Basic literature	J. Kalisz Podstawy elektroniki cyfrowej, WKiŁ 1998 J. Pieńkos, J. Turczyński Układy scalone TTL w systemach cyfrowych, WKiŁ 1986 Katalogi firmowe M. Barski, W. Jędruch Układy cyfrowe, podstawy projektowania i opis w języku VHDL, Wydawnictwo Politechniki Gdańskiej 2007 T. Łuba (red.) Synteza układów cyfrowych, WKiŁ 2003 Zasoby Internetu
	Supplementary literature	No requirements
	eResources addresses	Adresy na platformie eNauczanie:
Example issues/ example questions/ tasks being completed		
Work placement	Not applicable	