GDAŃSK UNIVERSITY OF TECHNOLOGY

Subject card

Subject name and code	Programmable Circuits Engineering, PG_00047914		
Field of study	Electronics and Telecommunications		
Date of commencement of studies	October 2024	Academic year of realisation of subject	2025/2026
Education level	first-cycle studies	Subject group	Obligatory subject group in the field of study Subject group related to scientific research in the field of study
Mode of study	Full-time studies	Mode of delivery	at the university
Year of study	2	Language of instruction	Polish
Semester of study	4	ECTS credits	3.0
Learning profile	general academic profile	Assessment form	assessment
Conducting unit	Department of Microelectronic Systems -> Faculty of Electronics, Telecommunications and Informatics		
Name and surname of lecturer (lecturers)	Subject supervisor	dr inż. Miron Kłosowski	
	Teachers	dr inż. Miron Kłosowski	

Lesson types and methods of instruction	Lesson type	Lecture	Tutorial	Laboratory	Project	Seminar	SUM
	Number of study hours	15.0	0.0	30.0	0.0	0.0	45
	E-learning hours included: 0.0						

Learning activity and number of study hours	Learning activity	Participation in didactic classes included in study plan	Participation in consultation hours	Self-study	SUM
	Number of study hours	45	3.0	27.0	75

Subject objectives	The aim of the course is to provide students with the basic knowledge and skills in the design of digital electronic circuits using FPGA technology and VHDL. As a result, students will be prepared to work in companies producing electronic equipment using FPGAs and firms producing specialized EDA software.

Learning outcomes

Course outcome	Subject outcome	Method of verification
[K6_U07] can apply methods of process and function support, specific to the field of study	Student uses software supporting the design of complex logic circuits.	[SU1] Assessment of task fulfilment
[K6_U08] while identifying and formulating specifications of engineering tasks related to the field of study and solving these tasks, can:n- apply analytical, simulation and experimental methods,n- notice their systemic and non-technical aspects,n- make a preliminary economic assessment of suggested solutions and engineering work n	Student identifies problems with digital circuits by simulating them in VHDL.	[SU1] Assessment of task fulfilment
[K6_U04] can apply knowledge of programming methods and techniques as well as select and apply appropriate programming methods and tools in computer software development or programming devices or controllers using microprocessors or programmable elements or systems specific to the field of study	Student designs digital circuits using the VHDL hardware description language. Student implements and tests digital circuits in a real hardware environment based on FPGAs.	[SU1] Assessment of task fulfilment
[K6_W33] Knows programming languages and equipment description languages, as well as methods for the synthesis of combinational and sequential circuits and programmable systems	Student describes the properties of the hardware description languages. Student knows the basics of the VHDL language. Student understands the processes of synthesis and simulation. Student is able to determine the conditions for the synthesis of the code in VHDL. Student describes the architecture and applications of SPLD, CPLD and FPGA programmable circuits. Student discusses methods of FPGA configuration.	[SW1] Assessment of factual knowledge
[K6_U09] can carry out a critical analysis of the functioning of existing technical solutions and assess these solutions, as well as apply experience related to the maintenance of technical systems, devices and facilities typical for the field of studies, gained in the professional engineering environment	Student analyzes sample digital systems and proposes the use of programmable circuits in systems currently implemented with other techniques.	[SU2] Assessment of ability to analyse information

Subject contents

1. Introduction to VHDL, its origin and applications. 2. Abstraction levels and description methods of digital circuits. 3. Design entity description in VHDL. 4. Assignments, signals, variables, operators. 5. Data types in VHDL. 6. Resolution function. 7. Vectors and operations on vectors. 8. Combinatorial processes. Synthesis of combinatorial logic. 9. Simulation and modelling in VHDL. 10. Conditional, case and loop statements in processes. 11. Constants and initial values of signals and variables. 12. Hierarchy and parametrization of design entities. 13. Sequential processes. 14. Synthesis of counters and frequency dividers. 15. Synthesis of shift registers. 16. State machines. State encoding. Forbidden states. 17. Meta-stability phenomenon and avoidance. 18. Attributes and their applications. 19. Type conversion in VHDL. 20. Functions and procedures in VHDL. 21. Implementation of logic functions in programmable circuits. 22. Configuration memory in programmable circuits. 23. Architecture and applications of SPLDs. 24. Architecture and applications of CPLDs. 25. Hardware description languages for SPLDs and CPLDs. 26. Architecture and applications of FPGAs. 27. Architecture and properties of input/output blocks in FPGAs. 28. Dedicated functional blocks in FPGAs. 29. Methods of functional block synthesis. 30. FPGA configuration methods. 31. Constrain driven design.

Prerequisites and co-requisites

Assessment methods and criteria

Subject passing criteria	Passing threshold	Percentage of the final grade
Practical exercise	50.0%	60.0%
Midterm colloquium	50.0%	40.0%

Recommended reading

Basic literature	Zwoliński Mark, "Projektowanie układów cyfrowych z wykorzystaniem języka VHDL", Wydawnictwa Komunikacji i Łączności WKŁ, Warszawa 2007.
Supplementary literature	No requirements
eResources addresses	Adresy na platformie eNauczanie:

Example issues/ example questions/ tasks being completed	Sample lab exercises: 1. Simple LED display driver. 2. PS/2 keyboard key-code readout. 3. Simple RS232 receiver and transmitter. 4. Video signal generator for VGA display.
Work placement	Not applicable