

## Subject card

Subject name and code	Digital Technology - laboratory, PG_00047557								
Field of study	Automatic Control, Cybernetics and Robotics								
Date of commencement of studies	October 2025		Academic year of realisation of subject			2025/2026			
Education level	first-cycle studies		Subject group			Obligatory subject group in the field of study			
					Subject group related to scientific research in the field of study				
Mode of study	Full-time studies		Mode of delivery			at the university			
Year of study	1		Language of instruction			Polish			
Semester of study	2		ECTS credits			4.0			
Learning profile	general academic profile		Assessmer	sment form			assessment		
Conducting unit	Department Of Automatic Control -> Faculty Of Electronics Telecommunications And Informatics -> Wydziały Politechniki Gdańskiej						tics ->		
Name and surname	Subject supervisor		dr inż. Marcin Pazio						
of lecturer (lecturers)	Teachers		dr inż. Marcin Pazio						
Lesson types and methods	Lesson type	Lecture	Tutorial	Laboratory	Projec	t	Seminar	SUM	
of instruction	Number of study hours	0.0	0.0	30.0	0.0		0.0	30	
	E-learning hours inclu	ours included: 0.0							
Learning activity and number of study hours	Learning activity	Participation in didactic classes included in study plan		Participation in consultation hours		Self-study		SUM	
	Number of study hours	30	4.0			66.0		100	
Subject objectives	The class of logic students acquire knowledge of:  The mathematical systems used to describe iterative combination and sequence combination  Introduction to binary, binary, Boolean algebra arytmetyka's logical functions  Basic concepts, systems, systems iterative  Synthesis of sequential iterative and sequence  Synthesis of synchronous and asynchronous sequential Circuits  memory								

IK6_U03  can design, according to required specifications, and make a simple device, facility, system or cardinations and make a simple device, facility, system or cand esign, according to the specification, and simple device, facility, system or dark of the field of study, using suitable methods and tools and specification, and make a simple device, object, system or specific to the field of study, using suitable methods and represent to the field of study, and experience gained in shuty and experience gained in the specific property price of study and experience gained in the specific property provided in the specific property provided and makerials, using standards and Engineering standards, using sterbriotopy; and makerials, using standards and Engineering activities.  Subject contents  OTTL and CMOS gates testing 2. Designing, assembling and testing synchronous sequential circuits for Assembling and testing synchronous sequential circuits. Designing counter modules 7. Assembling and testing counter modules 8. Designing, assembling and testing synchronous sequential circuits of Designing, assembling and testing synchronous sequential circuits 1. Assembling and testing caysnchronous sequential circuits 1. Assembling and testing synchronous sequential circuits 1. Assembling and testing system of modules 8. Designing, assembling and testing system of modules 8. Designing, assembling and testing system of testing circuits 2. Assembling and testing system of testing circuits 2. Assembling projects from ex. 13. 13. Prototyping digital circuits 5. Assembling and testing system of testing circuits 5. Assembling and testing system of testing and co-requisites  No requirements  Assessment methods and correct property of the specific projects from ex. 13. 15. Prototyping digital circuits 5. Assembling and correct projects from ex. 14. Assembling projects from ex. 13. 15. Prototyping digital circuits 5. Assembling and correct projects from ex. 14. Assembling projects from ex. 15. Design the specific projects from ex.	Learning outcomes	Course outcome	Subject outcome	Method of verification				
Designing and assembling digital timing circuits 4. Designing synchronrous sequential circuits 5. Assembling and testing synchronous sequential circuits 6. Designing counter modules 7. Assembling and testing counter modules 8. Designing, assembling and testing register modules 9. Designing asynchronous sequential circuits 10. Assembling and testing asynchronous sequential circuits 11. Microprogramming: coding data interchange between digital modules 12. Microprogramming: implementing the code from ex.11 13. Prototyping digital circuits designing various projects 14. Assembling projects from ex.13. 15. Prototyping: testing projects from ex.14.  Prerequisites  Assessment methods and criteria  Subject passing criteria passing threshold Percentage of the final grade activity / presence policy for presence policy for presence policy for presence passing threshold Realization of task policy for presence policy for pres		required specifications, and make a simple device, facility, system or carry out a process, specific to the field of study, using suitable methods, techniques, tools and materials, following engineering standards and norms, applying technologies specific to the field of study and experience gained in the professional engineering	can design, according to the specified specification, and perform typical digital systems a simple device, object, system or process, using appropriately selected methods, techniques, tools and materials, using standards and Engineering standards, using technology-specific technologies and using the experience gained in an environment of professional					
Assessment methods and criteria    Subject passing criteria   Passing threshold   Percentage of the final grade activity / presence   50.0%   50.0%     Recommended reading   R. F. Tinder, Engineering Digital Design J. D. Daniels, Digital Design from Zero to One Texas Instruments, Digital Design Seminar M. Basic literature   R. F. Tinder, Engineering Digital Design J. D. Daniels, Digital Design from Zero to One Texas Instruments, Digital Design Seminar M. Barski, W. Jedruch, Digital Circuits W. Majewski, L. Ogical Circuits Zieliński C.: Fundamentals of Digital Circuit Design, Wydawnictwo Naukowe PWN, Warsaw 2003   logic circuits Stefan Sieklicki - script from the subject of Logical Circuits asks being completed   Carry out the operation (10101)2 x (101) 2) the result reported in the decimal system, asks being completed   Carry out the operation (10101)2 x (101) 2) the result reported in the decimal system, and the subject of trigger JK and D.   Design the synchronous presence or within binary digits given in the series in the number of ones is an even number other than zero, which should be indicated by setting the output in=1 for exactly one clock cycle.   Enter in the solution:   1. Graf and a table to access/exit created based on graph tables and minimum output   1. Uniton schematic diagram   1. Uniton	Subject contents	Designing and assembling digital timing circuits 4. Designing synchronous sequential circuits 5. Assembling and testing synchronous sequential circuits 6. Designing counter modules 7. Assembling and testing counter modules 8. Designing, assembling and testing register modules 9. Designing asynchronous sequential circuits 10. Assembling and testing asynchronous sequential circuits 11. Microprogramming: coding data interchange between digital modules 12. Microprogramming: implementing the code from ex.11 13. Prototyping digital circuits: designing						
activity / presence   50.0%   50.0%   50.0%     Realization of task   50.0%   50.0%   50.0%     Recommended reading   Basic literature   R. F. Tinder, Engineering Digital Design J. D. Daniels, Digital Design from Zero to One Texas Instruments, Digital Design from Zero to One Texas Instruments, Digital Design Seminar M. Barski, W. Jedruch, Digital Circuits W. Majewski, Logical Circuits Zieliński C.: Fundamentals Of Digital Circuit Design, Wydawnictwo Naukowe PWN, Warsaw 2003   Logical circuits Zieliński C.: Fundamentals of digital circuits design, Wydawnictwo Naukowe PWN, Warsaw 2003   Logical circuits Stefan Sieklicki - script from the subject of Logical Circuits Adresy na platformie eNauczanie:		No requirements						
activity / presence   50.0%	Assessment methods	Subject passing criteria	Passing threshold	Percentage of the final grade				
Recommended reading  Basic literature  R. F. Tinder, Engineering Digital Design J. D. Daniels, Digital Design from Zero to One Texas Instruments, Digital Design Seminar M. Barski, W. Jedruch. Digital Circuits V. Majewski, Logical Circuits Zieliński C.: Fundamentals of Digital Circuit Design, Wydawnictwo Naukowe PWN, Warsaw 2003  Supplementary literature  Logical Circuits Sieliński C.: Fundamentals of digital Circuits design, Wydawnictwo Naukowe PWN, Warsaw 2003  logic circuits Stefan Sieklicki - script from the subject of Logical Circuits easely example questions/ tasks being completed  - Carry out the operation (10101)2 x (101) 2) the result reported in the decimal system,  - The function f(d,c,b,a)= П (0, 3, 5, 8, 12, 14, (2,11,13)) achieved using a a multiplexer 4/1 and NAND Gates.  - Provide a table of trigger JK and D,  - Design the table in a logical network to build the NAND Gate  - Design the synchronous presence or within binary digits given in the series in the number of ones is an even number other than zero, which should be indicated by setting the output in=1 for exactly one clock cycle.  Enter in the solution:  1. Graf and a table to access/exit created based on graph tables and minimum  2. function triggers excitations for pursuing more bits of triggers JK  3. minimum output  4. function schematic diagram			-					
from Zero to One Texas Instruments, Digital Design Seminar M. Barski, W. Jedruch, Digital Circuits W. Majewski, Logical Circuits Zieliński C.: Fundamentals of Digital Circuits V. Majewski, Logical Circuits Zieliński C.: Fundamentals of Digital Circuits Design, Wydawnictwo Naukowe PWN, Warsaw 2003   Logical circuits Zieliński C.: Fundamentals of digital circuits design, Wydawnictwo Naukowe PWN, Warsaw 2003   logic circuits Zieliński C.: Fundamentals of digital circuits design, Wydawnictwo Naukowe PWN, Warsaw 2003   logic circuits Zieliński C.: Fundamentals of digital circuits design, Wydawnictwo Naukowe PWN, Warsaw 2003   logic circuits Zieliński C.: Fundamentals of digital circuits design, Wydawnictwo Naukowe PWN, Warsaw 2003   logic circuits Zieliński C.: Fundamentals of digital circuits design, Wydawnictwo Naukowe PWN, Warsaw 2003   logic circuits Zieliński C.: Fundamentals of digital circuits design, Wydawnictwo Naukowe PWN, Warsaw 2003   logic circuits Zieliński C.: Fundamentals of digital circuits design, Wydawnictwo Naukowe PWN, Warsaw 2003   logic circuits Zieliński C.: Fundamentals of digital circuits design, Wydawnictwo Naukowe PWN, Warsaw 2003   logic circuits Zieliński C.: Fundamentals of digital circuits design, Wydawnictwo Naukowe PWN, Warsaw 2003   logic circuits Zieliński C.: Fundamentals of digital circuits design, Wydawnictwo Naukowe PWN, Warsaw 2003   logic circuits Zieliński C.: Fundamentals of digital circuits design, Wydawnictwo Naukowe PWN, Warsaw 2003   logic circuits Zieliński C.: Fundamentals of digital circuits design, Wydawnictwo Naukowe PWN, Warsaw 2003   logic circuits Zieliński C.: Fundamentals of digital circuits design, Wydawnictwo Naukowe PWN, Warsaw 2003   logic circuits Zieliński C.: Fundamentals of digital circuits design, wydawnictwo Naukowe PWN, Warsaw 2003   logic circuits Zieliński C.: Fundamentals of digital circuits design, wydawnictwo Naukowe PWN, Warsaw 2003   logic circuits Zieliński C.: Fundamentals of digital circuits Zieliński C.: Fundamentals of digital circui		Realization of task	50.0%	50.0%				
Wydawnictwo Naukowe PWN, Warsaw 2003   logic circuits Stefan Sieklicki - script from the subject of Logical Circuits	Recommended reading	from Zero to One Texas Instruments, Digital Design Seminar M. Barski, W. Jędruch, Digital Circuits W. Majewski, Logical Circuits Zieliński C .: Fundamentals of Digital Circuit Design, Wydawnictwo						
Example issues/ example questions/ tasks being completed  - Carry out the operation (10101)2 x (101) 2) the result reported in the decimal system,  - The function f(d,c,b,a)= Π (0, 3, 5, 8, 12, 14, (2,11,13)) achieved using a a multiplexer 4/1 and NAND Gates.  - Provide a table of trigger JK and D,  - Design the table in a logical network to build the NAND Gate  - Design the synchronous presence or within binary digits given in the series in the number of ones is an even number other than zero, which should be indicated by setting the output in=1 for exactly one clock cycle.  Enter in the solution:  1. Graf and a table to access/exit created based on graph tables and minimum 2. inmimum output 3 minimum output 4. function schematic diagram		Supplementary literature	Wydawnictwo Naukowe PWN, Warsaw 2003					
Example issues/ example questions/ tasks being completed  - Carry out the operation (10101)2 x (101) 2) the result reported in the decimal system,  - The function f(d,c,b,a)= Π (0, 3, 5, 8, 12, 14, (2,11,13)) achieved using a a multiplexer 4/1 and NAND Gates.  - Provide a table of trigger JK and D,  - Design the table in a logical network to build the NAND Gate  - Design the synchronous presence or within binary digits given in the series in the number of ones is an even number other than zero, which should be indicated by setting the output in=1 for exactly one clock cycle.  Enter in the solution:  1. Graf and a table to access/exit created based on graph tables and minimum function triggers excitations for pursuing more bits of triggers JK minimum output function schematic diagram		- Danish and danish						
- Carry out the operation (10101)2 x (101) 2) the result reported in the decimal system,  - Carry out the operation (10101)2 x (101) 2) the result reported in the decimal system,  - The function f(d,c,b,a)= Π (0, 3, 5, 8, 12, 14, (2,11,13)) achieved using a a multiplexer 4/1 and NAND Gates.  - Provide a table of trigger JK and D,  - Design the table in a logical network to build the NAND Gate  - Design the synchronous presence or within binary digits given in the series in the number of ones is an even number other than zero, which should be indicated by setting the output in=1 for exactly one clock cycle.  Enter in the solution:  1. Graf and a table to access/exit created based on graph tables and minimum function triggers excitations for pursuing more bits of triggers JK minimum output function schematic diagram		eResources addresses	Adresy na platformie eNauczanie:					
- Design the table in a logical network to build the NAND Gate  - Design the synchronous presence or within binary digits given in the series in the number of ones is an even number other than zero, which should be indicated by setting the output in=1 for exactly one clock cycle.  Enter in the solution:  1. Graf and a table to access/exit created based on graph tables and minimum 2. function triggers excitations for pursuing more bits of triggers JK 3. minimum output 4. function schematic diagram	example questions/							
- Design the synchronous presence or within binary digits given in the series in the number of ones is an even number other than zero, which should be indicated by setting the output in=1 for exactly one clock cycle.  Enter in the solution:  1. Graf and a table to access/exit created based on graph tables and minimum 2. function triggers excitations for pursuing more bits of triggers JK 3. minimum output 4. function schematic diagram		-Provide a table of trigger JK and D ,						
even number other than zero, which should be indicated by setting the output in=1 for exactly one clock cycle.  Enter in the solution:  1. Graf and a table to access/exit created based on graph tables and minimum 2. function triggers excitations for pursuing more bits of triggers JK 3. minimum output 4. function schematic diagram		- Design the table in a logical network to build the NAND Gate						
Graf and a table to access/exit created based on graph tables and minimum     function triggers excitations for pursuing more bits of triggers JK     minimum output     function schematic diagram		even number other than zero, which should be indicated by setting the output in=1 for exactly one clock						
function triggers excitations for pursuing more bits of triggers JK     minimum output     function schematic diagram		Enter in the solution:						
Work placement Not applicable		function triggers excitations for pursuing more bits of triggers JK     minimum output						
	Work placement	Not applicable						

Document generated electronically. Does not require a seal or signature.

Data wygenerowania: 24.04.2025 17:36 Strona 2 z 2