GDAŃSK UNIVERSITY OF TECHNOLOGY

Subject card

Subject name and code	Digital Technology I, PG_00067325		
Field of study	Technika cyfrowa I		
Date of commencement of studies	October 2025	Academic year of realisation of subject	2025/2026
Education level	first-cycle studies	Subject group	Obligatory subject group in the field of study Subject group related to scientific research in the field of study
Mode of study	Full-time studies	Mode of delivery	at the university
Year of study	1	Language of instruction	Polish
Semester of study	1	ECTS credits	6.0
Learning profile	general academic profile	Assessment form	exam
Conducting unit	Department of Signals and Systems -> Faculty of Electronics Telecommunications and Informatics -> Faculties of Gdańsk University of Technology		
Name and surname of lecturer (lecturers)	Subject supervisor	dr inż. Paweł Raczyński	
	Teachers	dr inż. Paweł Raczyński inż. Damian Kąkol dr inż. Krzysztof Cisowski dr inż. Marcin Pazio	

Lesson types

Lesson type	Lecture	Tutorial	Laboratory	Project	Seminar	SUM
Number of study hours	30.0	30.0	0.0	0.0	0.0	60

E-learning hours included: 0.0

eNauczanie source addresses:
Moodle ID: 2101 Technika cyfrowa I
https://enauczanie.pg.edu.pl/2025/course/view.php?id=2101

Learning activity and number of study hours

Learning activity	Participation in didactic classes included in study plan	Participation in consultation hours	Self-study	SUM
Number of study hours	60	6.0	84.0	150

Subject objectives

The aim of the course is to learn the mathematical description and the methods of analysis and design of digital integrated curcuits

Learning outcomes

Course outcome	Subject outcome	Method of verification
[K6_W03] knows and understands, to an advanced extent, the construction and operating principles of components and systems related to the field of study, including theories, methods and complex relationships between them and selected specific issues - appropriate for the curriculum	They can independently develop a concept for a designed digital system, select the appropriate functional blocks needed for its implementation, and properly connect them. They can also launch and test the designed digital system.	[SW3] Ocena wiedzy zawartej w opracowaniu tekstowym i projektowym [SW1] Ocena wiedzy faktograficznej
[K6_U03] can design, according to required specifications, and make a simple device, facility, system or carry out a process, specific to the field of study, using suitable methods, techniques, tools and materials, following engineering standards and norms, applying technologies specific to the field of study and experience gained in the professional engineering environment	339/5000 Is able to independently analyze the combined and sequential digital system. He can go from his scheme to the formal description. Is able to independently design a combination or sequential digital circuit in the optimal version. He can make the technical implementation of the designed system taking into account different technologies.	[SU1] Ocena realizacji zadania [SU2] Ocena umiejętności analizy informacji [SU4] Ocena umiejętności korzystania z metod i narzędzi

Subject contents	Course content – lecture 1. Basic concepts, combinational and sequential circuits. 2. Mathematical description of digital circuits function tables, logical functions, automata, graphs, and transition/output tables. 3. Binary system, binary arithmetic, BIN, HEX, BCD, U1, U2 codes. 4. Boolean algebra, axioms, definitions, and theorems. 5. Logical functions, canonical forms, NPS and NPI. 6. Minimization of logical functions, Karnaugh and McCluskey table methods. 7. Synthesis of combinational circuits using AND, OR, NOT, NAND, and NOR functors. 8. Typical combinational circuits. 9. Synthesis of combinational circuits using multiplexers, mixed structures. 10. Iterative circuits, trade-off between circuit complexity and propagation time. 11. Synthesis of synchronous sequential circuits abstract synthesis, minimizing the number of internal states, state coding, types of flip-flops and their use, methods of triggering flip-flops, combinational synthesis of sequential circuits. 12. Analysis of sequential circuits, conversion between Moore and Mealye models. 13. Synthesis of asynchronous sequential circuits, differences from synchronous circuits, abstract synthesis, state coding, critical and noncritical race conditions, race protection, implementation of asynchronous circuits using SR asynchronous flip-flops and combinational circuits with feedback, protection against static and dynamic hazards. 14. Technical synthesis of digital circuits gates, flip-flops, MSI circuits implementation technologies (bipolar and CMOS), parameters and characteristics, gates with OC and TS outputs, principles of circuit interconnection. 15. Typical sequential MSI circuits, counters, registers and their typical applications, bus organization in OC and TS techniques, addressing and synchronization problems. 16. Selected digital circuits: monostable and astable flip-flops, ROM memories (ROM, PROM, EPROM, EEPROM, and PLA) and their parameters and use in implementing logical functions. Course content – exercises 1. Basic concepts, combinational and sequential circuits. 2. Mathematical description of digital circuits function tables, logical functions, automata, graphs, and transition/output tables. 3. The binary system, binary arithmetic, BIN, HEX, BCD, U1, U2 codes. 4. Logical functions, canonical forms, NPS and NPI. 5. Minimization of logical functions, Karnaugh and McCluskey table methods.

	6. Synthesis of combinational circuits using AND, OR, NOT, NAND, and NOR functors. 7. Synthesis of combinational circuits using multiplexers, mixed structures. 8. Synthesis of iterative circuits. 9. Synthesis of synchronous sequential circuits abstract synthesis, minimizing the number of internal states, state coding, types of flip-flops and their use, methods of triggering flip-flops, combinational synthesis of sequential circuits. 10. Analysis of sequential circuits, conversion between Moore and Mealye models. 11. Synthesis of asynchronous sequential circuits, differences from synchronous circuits, abstract synthesis, state coding, critical and noncritical race conditions, race protection, implementation of asynchronous circuits using SR asynchronous flip-flops and combinational feedback circuits, protection against static and dynamic hazards.
Prerequisites and co-requisites	No requirements
Assessment methods and criteria	

Subject passing criteria	Passing threshold	Percentage of the final grade
open test examination	51.0%	40.0%
2 classworks for 20 points each, test for 30 point, possibitity to correct score with any subset of items at exam session	51.0%	60.0%

Recommended reading	Basic literature	J. Kalisz Podstawy elektroniki cyfrowej, WKiŁ 1998. J. Pieńkos, J. Turczyński Układy scalone TTL w systemach cyfrowych, WKiŁ 1986 Katalogi firmowe. M. Barski, W. Jędruch Układy cyfrowe, podstawy projektowania i opis w języku VHDL, Wydawnictwo Politechniki Gdańskiej 2007. T. Łuba (red.) Synteza układów cyfrowych, WKiŁ 2003 Zasoby Internetu.
	Supplementary literature	No requirements
	eResources addresses	
Example issues/ example questions/ tasks being completed		
Practical activites within the subject	Not applicable	

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