GDAŃSK UNIVERSITY OF TECHNOLOGY

Subject card

Subject name and code	Modelling and Simulation Languages , PG_00047822		
Field of study	Biomedical Engineering		
Date of commencement of studies	October 2025	Academic year of realisation of subject	2027/2028
Education level	first-cycle studies	Subject group	Optional subject group Subject group related to scientific research in the field of study
Mode of study	Full-time studies	Mode of delivery	at the university
Year of study	3	Language of instruction	Polish
Semester of study	5	ECTS credits	5.0
Learning profile	general academic profile	Assessment form	exam
Conducting unit	Department Of Microelectronic Systems -> Faculty Of Electronics Telecommunications And Informatics -> Wydziały Politechniki Gdańskiej		
Name and surname of lecturer (lecturers)	Subject supervisor	dr hab. inż. Bogdan Pankiewicz	
	Teachers	dr hab. inż. Bogdan Pankiewicz	

Lesson types and methods of instruction

Lesson type	Lecture	Tutorial	Laboratory	Project	Seminar	SUM
Number of study hours	30.0	0.0	30.0	0.0	0.0	60

E-learning hours included: 0.0

Learning activity and number of study hours

Learning activity	Participation in didactic classes included in study plan	Participation in consultation hours	Self-study	SUM
Number of study hours	60	5.0	60.0	125

Subject objectives

The aim of the subject is learning of modeling and simulation of electronic circuits using PSPICE and HDL languages such as Verilog and VHDL.

Learning outcomes

Course outcome	Subject outcome	Method of verification
[K6_U04] can apply knowledge of programming methods and techniques as well as select and apply appropriate programming methods and tools in computer software development or programming devices or controllers using microprocessors or programmable elements or systems specific to the field of study	Student can perform simulation using the PSPICE simulator. Student is able to design simple digital systems using Verilog and VHDL. The student is able to implement simple digital systems using FPGAs.	[SU1] Assessment of task fulfilment
[K6_W04] knows and understands, to an advanced extent, the principles, methods and techniques of programming and the principles of computer software development or programming devices or controllers using microprocessors or programmable elements or systems specific to the field of study, and organisation of systems using computers or such devices	Student knows the syntax of PSPICE files, types of possible simulations, ways of describing analog and digital circuits, and how to perform simulations of electronic circuits. Student knows HDL languages: Verilog and VHDL. Student is able to perform a description of the digital system and its simulation.	[SW1] Assessment of factual knowledge

Subject contents

1. Introduction to and applications of HDL languages. Genesis of Verilog language. 2. Abstraction levels (Verilog). 3. Design methodologies. Simple example. 4. Syntax of Verilog. 5. Data types. 6. System tasks and compilers directives. 7. Modules and ports. 8. Modelling at gate level. 9. Delays in gates. 10. Modelling at register level. 11. Concurrent assignment. 12. Expressions and operators. 13. Modeling at behavioral level. 14. Functions and tasks. 15. Modelling techniques. 16. Verilog 2001 changes in the standard. 17. Genesis of VHDL language. 18. Syntax and data types. 19. Entities and their architectures. 20. Instantiation of components. 21. Concurrent assignments, simple and conditional. 22. Delays, concurrent and time operations. 23. Processes. 24. Conditional commands and loops. 25. Delays with wait keyword. 26. Functions and procedures. 27. Libraries and packages. 28. IEEE library. 29. Synthesis of state machines. 30. Testing the design. 31. Other HDL languages.

<table>
<tr><td>Prerequisites and co-requisites</td><td colspan="3">No requirements</td></tr>
<tr><td>Assessment methods and criteria</td><td colspan="3"><table>
<tr><th>Subject passing criteria</th><th>Passing threshold</th><th>Percentage of the final grade</th></tr>
<tr><td>Exam</td><td>50.0%</td><td>50.0%</td></tr>
<tr><td>Practical exercise</td><td>50.0%</td><td>50.0%</td></tr>
</table></td></tr>
<tr><td rowspan="3">Recommended reading</td><td>Basic literature</td><td colspan="2">K.Skahill, Vhdl for Programmable Logic, Addison-Wesley Publishing Company, 1996. S.Palnitkar, Verilog HDL, SunSoft Press, 1996. M. Zwoliński, Projektowanie układów cyfrowych z wykorzystaniem języka VHDL, W.KiŁ, 2002.</td></tr>
<tr><td>Supplementary literature</td><td colspan="2">No requirements</td></tr>
<tr><td>eResources addresses</td><td colspan="2">Adresy na platformie eNauczanie:</td></tr>
<tr><td>Example issues/ example questions/ tasks being completed</td><td colspan="3"></td></tr>
<tr><td>Work placement</td><td colspan="3">Not applicable</td></tr>
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