GDAŃSK UNIVERSITY OF TECHNOLOGY

Subject card

Subject name and code	Logical Circuits, PG_00047361		
Field of study	Electronics and Telecommunications		
Date of commencement of studies	October 2026	Academic year of realisation of subject	2026/2027
Education level	first-cycle studies	Subject group	Obligatory subject group in the field of study Subject group related to scientific research in the field of study
Mode of study	Full-time studies	Mode of delivery	at the university
Year of study	1	Language of instruction	Polish
Semester of study	1	ECTS credits	4.0
Learning profile	general academic profile	Assessment form	exam
Conducting unit	Department of Automatic Control -> Faculty of Electronics Telecommunications and Informatics -> Faculties of Gdańsk University of Technology		
Name and surname of lecturer (lecturers)	Subject supervisor	dr inż. Marcin Pazio	
	Teachers	mgr inż. Tomasz Nowak dr inż. Marcin Pazio mgr inż. Marek Grzegorek	

Lesson types	Lesson type	Lecture	Tutorial	Laboratory	Project	Seminar	SUM
	Number of study hours	15.0	15.0	0.0	0.0	0.0	30
	E-learning hours included: 0.0						

Learning activity and number of study hours	Learning activity	Participation in didactic classes included in study plan	Participation in consultation hours	Self-study	SUM
	Number of study hours	30	4.0	66.0	100

Subject objectives

The class of logic students acquire knowledge of:

- The mathematical systems used to describe iterative combination and sequence combination

- Introduction to binary, binary, Boolean algebra arytmetyka's logical functions

- Basic concepts, systems, systems iterative

- Synthesis of sequential iterative and sequence

- Synthesis of synchronous and asynchronous sequential Circuits

- memory

Learning outcomes

Course outcome	Subject outcome	Method of verification
[K6_U08] while identifying and formulating specifications of engineering tasks related to the field of study and solving these tasks, can:n- apply analytical, simulation and experimental methods,n- notice their systemic and non-technical aspects,n- make a preliminary economic assessment of suggested solutions and engineering work n	The student of the Logic Systems can use the knowledge in the identification and formulation of engineering tasks related to the field of study and their solution: - use analytical, simulation and experimental methods, - recognize their system and non-technical aspects, - make a preliminary technical assessment of proposed solutions for electronic systems and undertaken engineering activities	[SU4] Assessment of ability to use methods and tools

Subject contents

Course content – lecture
1. Aims of the course (effects of the course): Skills of digital and microprocessor system description, analysis and designing with use of IC catalogues and application notes. 2. Description of CCs: logic functions and truth tables, description of SCs: state transition tables and diagrams for Moore and Mealy models. Examples of CCs and SCs circuits.Positional number systems: decimal, binary, octal, hexadecimal. 3. Signed number representation BIN, HEX, BCD, U1, U2, and binary arithmetic, floating-point notation. 4. SOP, POS and canonical forms of logic functions forms, other Algebras examples, exemplary uses of Boo-lean Algebra connecting networks 5. Simplification of logic functions using Karnaugh tables and, Quine-McCluskey methode . 6. CC design with logic gates AND, OR, NOT,NAND and NOR. Some remarks on simplification of SOP and POS forms contrary global simplification, transition times.

Prerequisites and co-requisites

No requirements

Assessment methods and criteria

Subject passing criteria	Passing threshold	Percentage of the final grade
activity / presence	50.0%	10.0%
Midterm colloquium	50.0%	50.0%
Written exam	50.0%	40.0%

Recommended reading

Basic literature	R. F. Tinder, Engineering Digital Design J. D. Daniels, Digital Design from Zero to One Texas Instruments, Digital Design Seminar
Supplementary literature	R. F. Tinder, Engineering Digital Design
eResources addresses	

Example issues/ example questions/ tasks being completed

- Carry out the operation (10101)2 x (101) 2) the result reported in the decimal system,

- The function f(d,c,b,a)= Π (0, 3, 5, 8, 12, 14, (2,11,13)) achieved using a a multiplexer 4/1 and NAND Gates.

-Provide a table of trigger JK and D ,

- Design the table in a logical network to build the NAND Gate

- Design the synchronous presence or within binary digits given in the series in the number of ones is an even number other than zero, which should be indicated by setting the output in=1 for exactly one clock cycle.

Enter in the solution:

1. Graf and a table to access/exit created based on graph tables and minimum
2. function triggers excitations for pursuing more bits of triggers JK
3. minimum output
4. function schematic diagram

Practical activites within the subject

Not applicable

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