GDAŃSK UNIVERSITY OF TECHNOLOGY

Subject card

Subject name and code	Programmable Digital Circuits, PG_00055352		
Field of study	Electronics and Telecommunications		
Date of commencement of studies	October 2026	Academic year of realisation of subject	2027/2028
Education level	second-cycle studies	Subject group	Obligatory subject group in the field of study Subject group related to scientific research in the field of study
Mode of study	Full-time studies	Mode of delivery	at the university
Year of study	2	Language of instruction	English
Semester of study	3	ECTS credits	2.0
Learning profile	general academic profile	Assessment form	assessment
Conducting unit	Department of Microelectronic Systems -> Faculty of Electronics Telecommunications and Informatics -> Faculties of Gdańsk University of Technology		
Name and surname of lecturer (lecturers)	Subject supervisor	dr inż. Piotr Kurgan	
	Teachers	dr inż. Piotr Kurgan	

Lesson types

Lesson type	Lecture	Tutorial	Laboratory	Project	Seminar	SUM
Number of study hours	15.0	0.0	15.0	0.0	0.0	30
E-learning hours included: 0.0						

Learning activity and number of study hours

Learning activity	Participation in didactic classes included in study plan	Participation in consultation hours	Self-study	SUM
Number of study hours	30	4.0	16.0	50

Subject objectives

The aim of the course is to develop a specialist having advanced knowledge and skills in the design, verification, testing and commissioning of digital electronic systems using FPGA technology. Graduates are prepared to work in companies producing electronic equipment using FPGAs or developing specialized EDA software. They are also prepared to participate in research programs where FPGA technology is used.

Learning outcomes

Course outcome	Subject outcome	Method of verification
[K7_U02] can perform tasks related to the field of study as well as formulate and solve problems applying recent knowledge of physics and other areas of science	Student solves design tasks using advanced FPGA digital system design tools (IP-core generator, FPGA editor). Student uses advanced tools for digital FPGA system design (IP-core generator, FPGA editor). Student uses advanced tools to optimize digital FPGA systems (floorplanner).	[SU1] Assessment of task fulfilment
[K7_W02] knows and understands, to an increased extent, selected laws of physics and physical phenomena, as well as methods and theories explaining the complex relationships between them, constituting advanced general knowledge in the field of technical sciences related to the field of study	The student knows the physical principles of operation of digital circuits and the physical foundations of configuration memories used in digital programmable circuits.	[SW1] Assessment of factual knowledge
[K7_U04] can apply knowledge of programming methods and techniques as well as select and apply appropriate programming methods and tools in computer software development or programming devices or controllers using microprocessors or programmable elements or systems specific to the field of study, making assessment and critical analysis of the prepared software as well as a synthesis and creative interpretation of information presented with it	Student uses advanced mechanisms of the VHDL and Verilog languages. Student uses the SystemC environment. Student implements FPGA digital circuits using advanced tools. Student uses mechanisms of constrain driven design in synthesis and implementation. Student uses IP-core modules. Student designs systems with multiple clock domains.	[SU1] Assessment of task fulfilment
[K7_W04] knows and understands, to an increased extent, the principles, methods and techniques of programming and the principles of computer software development or programming devices or controllers using microprocessors or other elements or programmable devices specific to the field of study, and organization of work of systems using computers or such devices	Student describes advanced mechanisms of VHDL and Verilog languages. Student knows the basics of the SystemC environment. Student knows the basic issues of optimization of digital systems.	[SW1] Assessment of factual knowledge

Subject contents

Course content – lecture
1. Advanced topics of VHDL and Verilog in digital circuit synthesis. 2. Introduction to SystemC. 3. Project constraining methods. 4. Timing constraints. 5. Software tool for timing analysis. 6. Synthesis constraints and optimization. 7. "Place and route" process constraints and optimization. 8. Floorplanner software tool. 9. Other constraints. 10. Clock management in FPGA. 11. Design of FPGA systems with multiple clock domains. 12. Design of reset circuits. 13. Source-synchronous and system-synchronous timing. 14. Implementation of asynchronous circuits using FPGA. 15. IP-core blocks in FPGA systems. 16. FPGA manual configuration modification. 17. FPGA editor software tool. 18. FPGA circuits with embedded processor. 19. Soft-core processors for FPGA. 20. FPGA circuit diagnostics. 21. Error tolerance in FPGA systems. 22. FPGA circuits with FLASH configuration memory. 23. Mixed-signal programmable circuits. 24. FPGA circuits with anti-fuse technology. 25. Advanced methods of FPGA configuration. 26. In-system FPGA reconfiguration - methods and applications. 27. Security of intellectual property in FPGA systems. 28. FPGA to ASIC migration.

Prerequisites and co-requisites

Assessment methods and criteria

Subject passing criteria	Passing threshold	Percentage of the final grade
Midterm colloquium	50.0%	30.0%
Practical exercise	50.0%	70.0%

Recommended reading

Basic literature	1. Steve Kilts, "Advanced FPGA Design - Architecture, Implementation and Optimization", John Wiley & Sons, Inc., 2007. 2. Zwoliński Mark, "Projektowanie układów cyfrowych z wykorzystaniem języka VHDL", Wydawnictwa Komunikacji i Łączności WKŁ, Warszawa 2007.
Supplementary literature	No requirements
eResources addresses	

Example issues/ example questions/ tasks being completed

Practical activites within the subject	Not applicable

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